

Product Brief

Multi-protocol, High-speed SERDES I/O Core

Highlights

- Designed in the Toshiba 90 nm process for smallest footprint and reduced cost
- Supply voltage of 1.2 volts with optional TX supply of 1.8 volts for higher output amplitudes
- Scalable for more than 64-ports of Fibre Channel
- Each receiver and each transmitter are independently programmable allowing for independent rate negotiation
- Hot-pluggable transceivers for improved reliability
- Calibrated 100 ohms differential I/Os for ease of connectivity
- Low system-power consumption with global as well as per-receiver and per-transmitter power-down modes
- Advanced multi-tap TX pre-emphasis and Rx equalization make interoperability with other system components possible without extra support
- Serial data rates and parallel interface datapath widths are programmable with both 8 and 10 (16 and 20) bit modes to enable support for both 8B/10B and non-8B/10B applications
- User configurable input/output data polarity gives greater degree of design freedom
- Spread Spectrum Clocking generation through the use of a clock generation module, also the receiver CDR can support programmable Spread Spectrum Clocking

Description

The Toshiba multi-protocol SERDES I/O core is a low-risk, silicon-proven solution for Fibre Channel 1/2/4/8 Gbps, 10-Gigabit Ethernet (4x XAUI), Serial ATA (SATA) 1.5/3.0 Gbps, Serial Attached SCSI (SAS) 1.5/3.0/6.0 Gbps and PCI-Express 2.5/5.0 Gbps applications. The multi-protocol SERDES cells allow rate negotiation on a per channel basis for mixed systems utilizing 1/2/4/8 Gbps Fibre Channel and 1.5/3.0/6.0 Gbps PCI-Express 2.5/5.0 Gbps SATA/SAS. The multi-protocol SERDES I/O core family of products makes it possible to obtain optimum form factors, while minimizing power consumption and enabling high-port densities. Toshiba Fibre Channel PHY cells support implementations of protocol controller, switch and disk drive ICs for applications including host bus adapters (HBAs), fabric, director edge and core switches and storage arrays.

The core maintains compatibility to legacy systems as it allows both Rx and Tx to operate at different data rates and to auto negotiate. In addition the core can handle legacy voltage levels up to 2V peak-to-peak differential output on the Tx and Rx cells.

Tight jitter performance allows for ease of support in SAS and SATA applications. Signal integrity requirements can be met in wirebond package solutions. The modular architecture consisting of multiple core hardmacros can be stacked allowing for denser channel configurations per die.

The programmable dual loop Tx CDR is suitable for repeater and timing applications. In addition, the 3-tap pre-emphasis in the Tx along with the 2 stage Rx equalization allows for a greater degree of freedom.

Features

Transmitter

- Differential CML outputs with programmable edge rate control
- Fully programmable multi-tap transmitter pre-emphasis
- Adjustable output drive levels to minimize power and crosstalk
- Transmitter can generate 2^7-1 PRBS or programmable data pattern

Receiver

- Differential CML signaling operates with AC coupled inputs
- Two-stage receiver equalization, each stage is 6-bit programmable, providing 0–10 dB gain
- Configurable Rx CDR supporting Spread Spectrum Clocking
- RX LOS detector
- PRBS pattern checker
- Programmable word alignment of RX recovered parallel data
- Detects loss of reference clock and loss of lock

Reference Clock

- Supports 50 MHz to 450 MHz input clock rate
- On-chip 100 ohm differential termination eliminates the need for an external resistor
- Three reference clock inputs for multi-clock/multi-standard support
- Detect loss of reference clock and loss of lock

Fibre Channel and other Standards Support

- Support for 1.0625 Gbps, 2.125 Gbps, 4.25 Gbps and 8.5 Gbps Fibre Channel
- Support for 3.1875 10-Gigabit Ethernet
- Support for 1.5 and 3.0 Gbps SATA

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- Support for 1.5, 3.0 and 6.0 Gbps SAS
- Support for 2.5 and 5.0 Gbps PCI-Express

Test Support

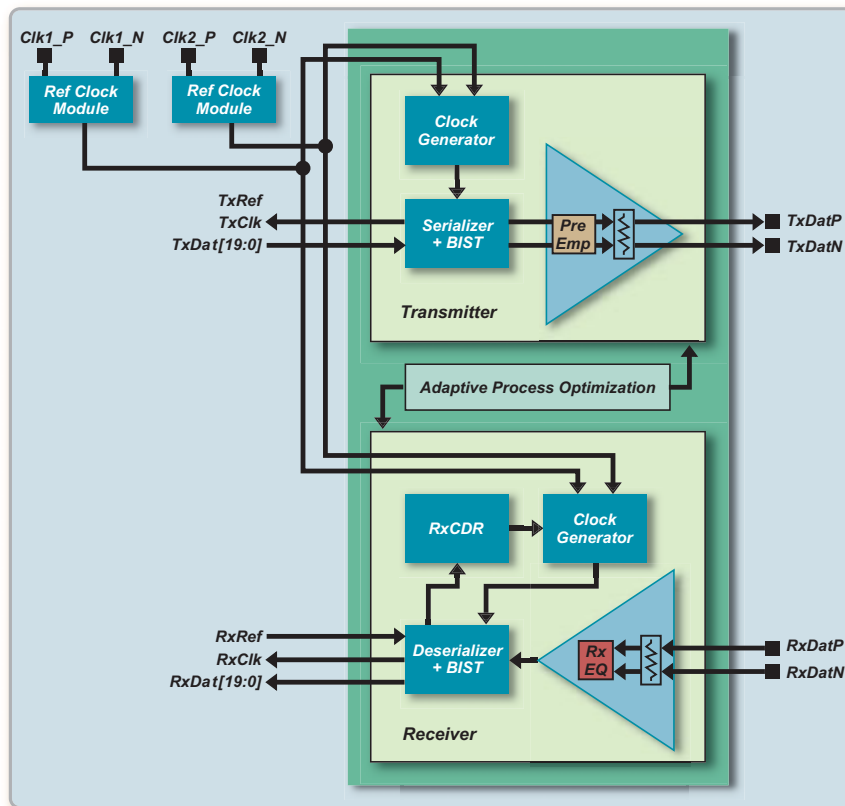
- Serial IO modules support internal scan
- Global power-down mode supports IDDQ and burn-in test methods
- IEEE 1149.1(DC) and 1149.6 (AC) JTAG boundary scan support
- Internal serial and parallel data loop back modes

- On-chip controller provides access to full array of internal proprietary control/status registers for device debug

Power Supplies and Packaging

- Supply voltage of 1.2 volts with optional TX supply of 1.8 volts for higher output amplitudes
- Support for Flip Chip BGA and wire bond packages

SERDES Serial I/O Core Block Diagram



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