

Toshiba RFCMOS ASIC: A Methodology for Successful RFCMOS SoC Implementation

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Highlights

- As the demand for high-speed, high-bandwidth portable applications has increased, there has been a corresponding increase in the number for RFCMOS designs.
- RFCMOS has traditionally been achieved through one of two design methodologies: two-chip system in package (SiP) or full-custom system-on-chip (SoC).
- While the SiP approach offers ease of integration, lower development cost and the use of mainstream manufacturing to produce it, high unit cost and long-term reliability are growing areas of concern. These concerns are addressed via implementation on an SoC, but the design and manufacturing complexities associated with single-chip RFCMOS can be daunting to most companies.
- The Toshiba RFCMOS ASIC reduces the design challenges and costs associated with RFCMOS thanks to the company's mature and stable processes, highly reputable IDM's support infrastructure and extensive experience with RFCMOS integration.

Introduction

The burgeoning market for high-speed, high-bandwidth portable communications products is creating unprecedented demand for RFCMOS solutions. From nearline applications such as home networking, Bluetooth, and RFID for distances less than three meters, to 802.11a/b/g and local area network products spanning up to 100 meters, to wide area networking solutions such as WIMAX, all aspects of the wireless communications market are on the rise. Along with this rapid growth comes increasing demand for the cost, power and density benefits of integrated CMOS, analog and RF devices.

Several options for implementing an RFCMOS solution exist today, each of which has its advantages and disadvantages. However, when critical design considerations, such as performance/power trade-off, design risk, reliability, time to market and unit price are taken into account, traditional solutions start to run out of steam.

Until now, companies have chosen primarily between two different RFCMOS implementation alternatives: a two-chip system-in-package (SiP), or a single-chip, full-custom system-on-chip (SoC). These approaches offer benefits, but there are trade-offs, and the disadvantages can be significant. Toshiba's RFCMOS ASIC methodology for single-chip RFCMOS implementation represents a new approach that, when weighed against other methods, offers compelling advantages.

The two-chip SiP

A common implementation option for system designers intermixing RF and logic elements has been a two-chip SiP. In a SiP, the RF component is realized in analog RFCMOS, GaAs, SiGe BiCMOS or other technology, and the baseband processor is deployed in high density standard digital CMOS. Both chips are then tested separately, mounted on a common substrate and packaged as a single unit.

The advantages of the SiP approach have been ease of integration, low cost of development and the use of mainstream manufacturing to produce it. From a development perspective, it's relatively simple to either procure or design RF and/or analog components and implement logic in a standard ASIC or COT flow. For example, manufacturing costs can be minimized in a two-chip approach by building the radio component in a low-cost legacy process technology, such as BiCMOS and SiGe, optimized for power constraints, and the baseband element in standard CMOS technology. Specialized processing of the various components affords good performance, as well as low-power dissipation.

SiP is effective at achieving the desired functionality while keeping power and performance in check; however, unit cost and long-term reliability are issues that a growing number of companies are finding problematic. Over time, the savings in development effort afforded by the SiP approach is offset by high unit price due to the expensive dual-chip packaging it requires.

Reliability is also a concern with two-chip implementation. Indeed, failures in time (FITs)

have been proven to increase exponentially with the number of individual parts in a system. Factors like strenuous qualification environments and thermal and other stresses may induce failures such as opens or shorts in the connections between chips and chip cracking. Procurers of consumer-oriented communications devices now place strict limits on failure rates they will accept, so this liability of the two-chip system can present a significant problem.

Single-chip implementation

Given the unit cost and reliability concerns associated with SiP implementation, and the industry's relentless pursuit of integration, communications device makers have been eager to adopt single-chip RFCMOS solutions. Only recently did such solutions become feasible, though. With the advent of sub-130 nm process technology that yields both high unity gain frequency (ft) MOSFETs and tight process control, it is now possible to realize both active and passive components using the same process technology.

Consolidating RF, analog and logic onto one chip has long been a dream of the industry, but it does take some effort to achieve a single-chip design. The development cost and effort for an RFCMOS SoC is high compared to a comparable two-chip SiP. And, as radio frequency increases, so does the development effort. The use of a more sophisticated process technology can add to the complexity as well. The development cost can be offset over time by lower unit cost, though, and the reliability improvement alone makes the switch justifiable for many.

COT methodology

Another development model for RFCMOS SoCs has been the traditional, full-custom, or COT, model. In a COT flow, the developer contracts with a foundry and other third parties such as design houses, IP houses, packaging houses and qualification houses to design, fabricate, package and test its custom-designed SoC. The foundry provides a design kit that includes models for passive and active components, process design rules and basic libraries. The customer develops, or procures from third parties, all elements of the design, including any IP, SRAM, ROM, I/Os, ESD and latch-up structures, and then hands off GDSII layout based on the foundry's rules and design kit. The foundry manufactures and delivers untested or partially tested

wafers several weeks later, and the customer works with packaging and testing houses to get finished packaged units.

The COT flow gives the developer complete control of the design. The benefits to the developer are the high level of customization of the end product and the ability to retarget the design to another foundry. However, many have learned that there are significant risks associated with this classic methodology, and those risks are increasing.

In the fabless model, ownership and responsibility for problems that arise is unclear. For example, if a developer procures IP and the IP doesn't work or, worse, the IP company disappears, the developer is left high and dry trying to debug a block that he or she didn't even design in the first place. When bugs or functional/performance concerns arise, and they always do in today's complex ICs, the burden of proof and time to market risk falls in the hands of the developer.

Another risk of this approach has to do with new design considerations around design for manufacturability (DFM) and yield (DFY) below the 130 nm process node. Challenges such as Lithography Compliance Check, hot spot fixing and other physical design issues for SoCs at 90 nm and 65 nm require much closer interplay between designer and fabricator, and more design control by the manufacturer, than that of a pure-play foundry relationship. Even with SPICE models that reflect process variations, other factors such as clean power supplies and design tool inaccuracy can result in difficult verification issues. The risk is compounded by variations in packaging electrical constraints, such as variations in substrate impedance. It can take three to four costly and time-consuming respins to comprehend all of the factors that come into play, and turn out a working product.

Smaller companies and start-ups are particularly vulnerable to the risks of a COT flow. Large companies are the primary drivers of RFCMOS technology, and tend to get preferred access to custom process and libraries at pure-play foundries. Emerging companies, on the other hand, often find themselves at the mercy of library and process limitations of a generic technology. For example, start-ups wanting to enter into the mobile handsets market, even when working with a \$10 – 100M investment, have trouble competing with larger companies that have the massive dollars and resources to implement a single chip configuration with the

optimum package height, etc. Without these resources, and possibly relegated to lesser technology and a COT model, smaller companies' budgets and market opportunities quickly can be dashed with the repeated respins typical of COT designs. So, these startups chase the dream, but very few of them are able to get launched into market niches occupied by larger companies using a classic COT flow.

For technical reasons, the COT model is likely to become less and less viable at sub-130 nm geometries, and it is clear that another model is needed for the broad spectrum of suppliers. Developers seeking to realize the promise of RFCMOS technology need to adopt a methodology that allows for closer interaction with and between the manufacturer and other parties. In addition, with the size and complexity of today's chips, the developers need to hone their focus on design tasks to which they add significant value, such as the design of RF and analog elements and overall system architecture, leaving other implementation tasks to the Integrated Device Manufacturer (IDM). In these ways, the time-to-market and design risk of a traditional COT approach can be avoided, and design success assured.

Toshiba's RFCMOS ASIC methodology

With its single single-chip implementation and leading edge RFCMOS technology, Toshiba offers an advanced, low risk and highly productive methodology to developers of RFCMOS ASICs. Instead of serving as a pure-play foundry that provides arms-length support, Toshiba is an IDM providing value added design support, integration, comprehensive designs kits, all IP elements and the benefits of a true one-stop shop. In addition to comprehensive design support, the Toshiba RFCMOS ASIC flow offers access to Toshiba's advanced fabrication and packaging technologies.

Underlying the methodology is the Toshiba single-chip RFCMOS technology, available at the 130 nm, 90 nm and 65 nm process nodes. This technology combines Toshiba's mature baseline CMOS processes with a full-featured RF process module. The RF module enables on-chip integration of passive elements such as MIM or MOM capacitors, junction and MOSFET varactors (deep N-well, single-end and differential), inductors (half turn, differential or symmetrical), mid-range poly

resistors with zero temperature coefficients, and junction capacitors, as well as parasitic devices such as NPN transistors. Toshiba's 130 nm, 90 nm and 65 nm processes are characterized by high ft of ~90 GHz, 150+ GHz and 250+ GHz respectively. Detailed characterization reports on both active and passive devices are included in the design kit.

The design development phase of Toshiba's RFCMOS ASIC flow is actually comprised of two parallel flows – one for the digital baseband processor and the other for the analog/RF elements. For the digital portion of the chip, Toshiba accepts a gate-level netlist and implements the GDSII for the digital portion, as in a standard ASIC flow. (see Figure 1) Toshiba performs value-added place and route services that take into account DFM/DFY considerations. The customer gets real-time feedback at the macro cell level and can also view the placed and routed data in order to optimize verification prior to freezing the cell. This way, hot spots and defects are fixed prior to tape-out, potentially saving millions of dollars in fixed and opportunity costs.

For the analog elements, the customer implements the GDSII with Toshiba's involvement to ensure success in manufacturing. Toshiba provides a uniquely comprehensive design kit that includes not only standard ASIC libraries, SPICE DFM/DFY models and package parasitics, but also proven IP elements like USB, A/D, D/A, PLL, SRAM, ROM, I/O, ESD and latch-up structures. The customer applies its expertise to physical design of the value-added elements of the macro cell, and Toshiba actively provides feedback on process-dependent layout considerations. Once the macro cell layout is frozen, all manufacturability and yield-assurance rules will have been followed, and downstream respins are avoided.

After digital and analog elements are laid out, Toshiba's design team integrates them into a single SoC. The team also stitches in proven SRAM, I/O, latch-up or ESD structures, or ROM. After the SoC layout is complete, the customer signs it off based on verification reports provided by Toshiba.

To help validate a design prior to making the significant investment in production tooling, the Toshiba RFCMOS ASIC offering includes a "shuttle run" in which design blocks can be prototyped on a multi-project wafer. Thirty days prior to the quarterly fab start, customers can

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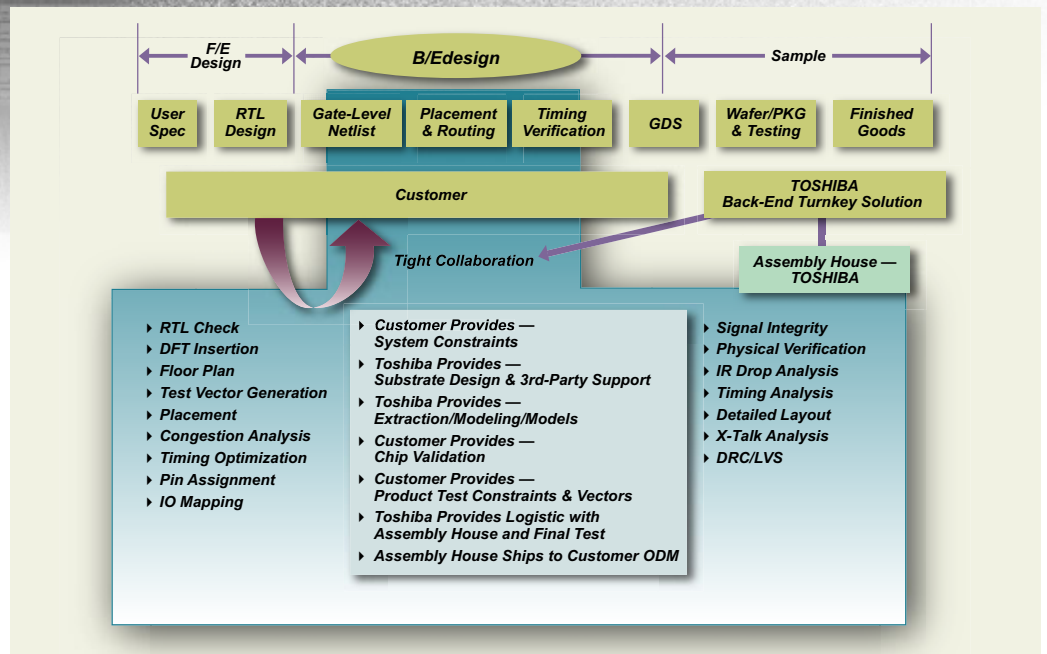


Figure 1. Flexible Interface Model

provide GDSII of an analog block, full new design, or existing design to be returned to Toshiba's process for second sourcing. Once the prototype is approved, a dedicated mask set is created.

To complete the turnkey RFCMOS offering, Toshiba performs its advanced packaging and testing services. The customer receives finished, packaged and tested units from a vendor that has carried the entire design from implementation through fabrication and packaging.

A superior solution for RFCMOS implementation

Toshiba's RFCMOS ASIC methodology offers distinct advantages over COT implementation. Developers benefit from the productivity and full power/performance benefits of a standard cell

implementation, along with a guided hand-off of custom mixed-signal content. Toshiba is intimately familiar with its process variations, tool limitations, static timing issues, cross talk, noise modeling, and is also an ASIC-savvy IDM, with proven core competency in IC development and manufacturing. A turnkey solution from such a provider assures clear ownership and virtually eliminates much of the design risk resulting from the involvement of multiple parties or an arms-length foundry.

The Toshiba RFCMOS ASIC methodology allows customers to take full advantage of mature and stable Toshiba processes and leverages a highly reputable IDM's support infrastructure and extensive experience integrating such SoCs in portable applications.

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