

Virtual Prototyping for a Custom SoC

Highlights

- Optimize the design margin at a very early stage of chip design
- Reduce turnaround time from several months to several weeks
- Zero re-spins due to power, signal integrity or package limitations
- Seamless integration of chip/package co-design within one tool

Description

Toshiba innovation now enables custom System-on-Chip (SoC) customers to view a Virtual Prototype long before design start. The Toshiba modern ASIC Virtual Prototyping system allows for the concurrent co-design of a chip, package and system. By using the Toshiba chip/package/system co-development methodology, designers can optimize their ASICs for cost and performance, shorten development turnaround time and dramatically increase the likelihood of a successful design in first pass silicon compared to less sophisticated methods of co-design.

This Virtual Prototyping System and verification tool enables an accurate assessment of the ASIC early on in the pipe-cleaning phase of the ASIC design. Typically, such designs are done in sequential fashion and inadequate margins are used by designers using “rule of thumb”

methodologies, thereby risking the project schedule and engineering re-design. This signoff, termed virtual model signoff, allows for a more confident place and route of the design and a DFM assured tape out.

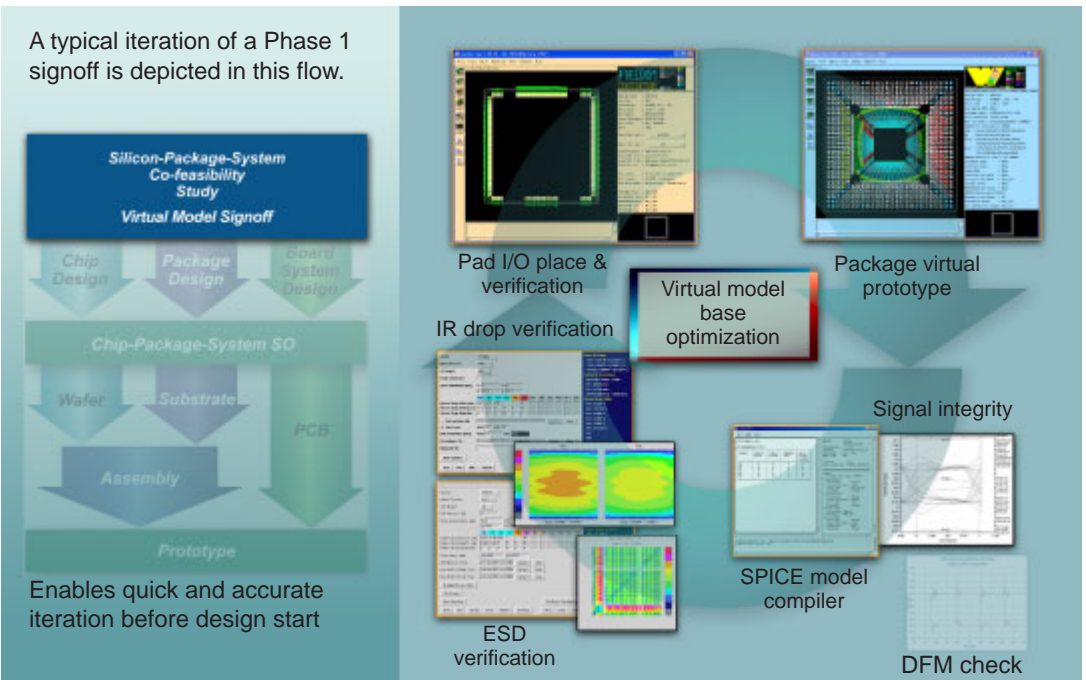
After customer netlist and constraints are provided to a Toshiba design center, Toshiba delivers a virtual prototype model and signoff in Phase 1 followed by a DFM assured Phase 2 of place and route GDSII data to the factory. A typical 10-week design flow for 65 nm and 90 nm designs includes the following steps:

Phase 1: First 5 weeks after design start

- View die/package virtual prototype
- Signal integrity check
- IR drop check
- Pad I/O placement and verification
- DFM checked
- Extracted SPICE/IBIS model from this prototype
- Virtual model signoff
- ESD verification

Virtual Model Optimization

A typical iteration of a Phase 1 signoff is depicted in this flow.



TAEC Regional Sales Offices

NORTHWEST

San Jose, CA

TEL: (408) 526-2400

FAX: (408) 526-2410

Portland, OR

TEL: (503) 784-8879

FAX: (503) 466-9729

SOUTHWEST

Irvine, CA

TEL: (949) 623-2900

FAX: (949) 474-1330

Richardson, TX

TEL: (972) 480-0470

FAX: (972) 235-4114

CENTRAL

Buffalo Grove, IL

TEL: (847) 484-2400

FAX: (847) 541-7287

NORTHEAST

Marlboro, MA

TEL: (508) 481-0034

FAX: (508) 481-8828

Parsippany, NJ

TEL: (973) 541-4715

FAX: (973) 541-4716

SOUTHEAST

Duluth, GA

TEL: (770) 931-3363

FAX: (770) 931-7602

www.Toshiba.com/taec

Phase 2: Next 5 weeks

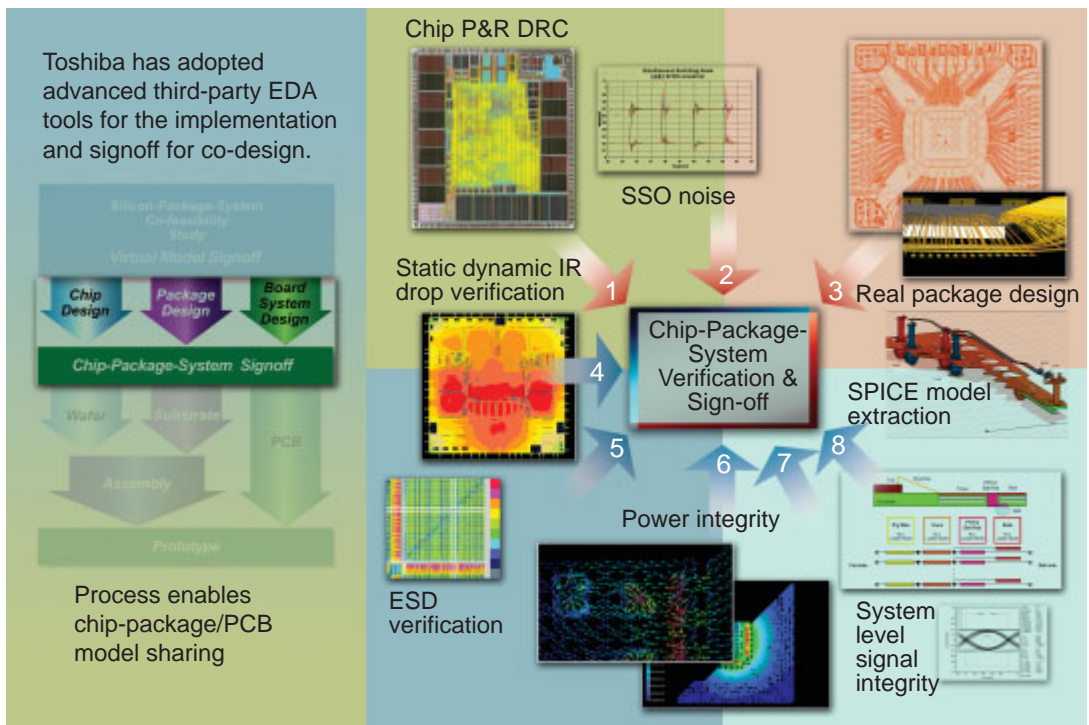
Some of the key steps of Phase 2 include:

- Chip P&R DRC
- SSO noise
- Real package design
- Static dynamic IR drop verification
- ESD verification
- Power integrity
- System level signal integrity
- SPICE model extraction

In essence, the Virtual Prototyping model signoff validates your design specifica-

tions by checking silicon and package integrity using a proven EDA toolset. In this signoff flow the package/device models and constraint information are read in from industry-standard third-party tools. The flow checks for the signal, IR, power and thermal integrity, in addition to ESD signoff, routability and bondability of the chosen package. This signoff is achieved within weeks of design start thereby eliminating many potential risks downstream. The signoff system includes these eight key subsystems:

Implementation and Signoff



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