Stacked 3D NAND flash memory promises to deliver higher performance and capacity.

**Q: What is 3D NAND?**
**A:** 3D NAND is a vertical implementation of the NAND flash cell memory array. The memory cell transistors forming the NAND string are connected in a series vertically and the memory transistors are changed from the floating-gate type to a trapped-charge type.

In floating-gate technology, die density is increased by shrinking peripheral circuits and active circuits. With 3D, holding the X/Y dimension of the die constant, die density is increased through multiple layers of the active circuits on the Z axis. Higher-density TLC 3D NAND die enables applications needing high-density NAND chip solutions.

**Q: What is the difference between bonded and through-silicon via (TSV) approaches?**
**A:** 3D technology typically employs one of two methods for connecting stacked die in a package (Fig. 1). One approach employs conventional wire-bonding techniques used with planar die to connect multiple die in a package. For high-density applications requiring high-speed I/O with reduced power consumption, the other approach is through-silicon via (TSV). This is similar to the through-holes used with printed circuit boards (PCBs).

Bonded connections are more limited since they must be placed around the periphery of the die. Stacked layers are more of a challenge when connections to the die are not common across the die. TSV connections can be placed anywhere on the die, allowing more flexibility in placement as well as numbers.

**Q: What are the main features and benefits of 3D NAND?**
**A:** Higher capacity storage is the main benefit of 3D NAND—but not the only one. Higher throughput, increased endurance, and improved power efficiency (while consuming less power) are some of the additional features and benefits of 3D NAND.

**Q: What is different about the controller used for 3D NAND flash versus floating gate (FG)?**
**A:** The controller architecture is basically the same, however some algorithm is optimized to enable 3D NAND flash features such as “one shot programming,” or full sequence programming, which enables three logical pages of data to be programmed in one programming cycle. This significantly boosts programming speed compared to floating-gate TLC flash.

**Q: How do increased layers affect the stacking challenge?**
**A:** Stacking layers is the most critical and challenging step in 3D NAND flash. Optimization of the memory hole size, memory hole pitch, sacrificial film, and stacking structure as well as evolution of dry etching technology will be necessary to increase the number of layers.

**Q: What mechanical issues face the industry moving from floating gate to 3D NAND flash?**
**A:** Because the stacked layers are formed on the surface of the wafer and the different materials used have different coefficients of thermal expansion, the wafer may warp during dielectric film, silicon film, or the metal layer deposition process due to tensile and compressive stress. These stress conditions are optimized and controlled at the deposition and cleaning process.

**Q: How does the gate technology change to support floating gate to 3D NAND flash?**
**A:** For 2D NAND, the stack-gate cell and the peripheral gate have similar structures with the active transistors sitting at the surface of the silicon.
wafer. In 3D NAND flash, the cells are stacked vertically with the memory cell transistors deposited on the top of the silicon wafer in multiple layers.

**Q:** Can 3D NAND die be stacked as well?
**A:** Yes. The approach of stacking die with 3D NAND is used frequently, especially in solid-state drives (SSDs), to further increase capacity.

**Q:** What is the impact of 3D NAND on the enterprise?
**A:** The enterprise storage appetite is insatiable. Anything that can provide more storage at lower prices and higher performance is desirable, so 3D NAND is one of the main delicacies on the plate. It provides higher densities, higher throughput, increased endurance, improved power efficiency while consuming less power, and is much faster than hard disk drives (although slower than DRAM and some other forms of flash memory). The favorable total cost of ownership (TCO) of deploying 3D NAND flash in enterprise storage is accelerating its presence in the enterprise as a replacement for hard disk drives (HDDs). Enterprise applications also impose their own requirements on storage that are often different and more robust than storage used for consumer-grade applications. Higher reliability is often preferred over high capacity.

**Q:** Are we reaching a limit on the number of layers that can be used in a single chip?
**A:** Not yet. The limit is set by the available technology that continues to improve. Sixty-four layers is a lot, for now.

**Q:** So what is next with 3D NAND?
**A:** More layers and improved connectivity are a given. The use of TSV technology will also lead to higher data rates and will provide an ideal solution for low latency, high bandwidth, and high IOPS/Watt in flash storage applications, including high-end enterprise SSDs. The move to quad-level cell (QLC) is the next step in cell density storage. The combination will continue the trend toward even denser storage systems.