

Description

The TMPR3927F is a 32-bit MIPS RISC microprocessor of the TX39 family. The TMPR3927F uses the TX39/H2 Processor Core as the CPU, which is a RISC CPU core Toshiba developed based on the MIPS® R3000A architecture. The TMPR3927F has built-in peripheral circuits such as a PCI Bus Controller, SDRAM Memory Controller, ROM Controller, DMA Controller, Interrupt Controller, Serial Communication Ports, Timer/Counter, and Parallel Port implementations.

Microprocessor Features

- Built-in TX39/H2 Processor Core
 - Developed based on the R3000A architecture
 - Instruction cache 8KB and Data cache 4KB
 - 2-way set associative Instruction/Data cache both supporting cache locking function
 - Supports write-through and write-back protocols in Data cache
 - Five-stage pipeline: Fetch, Decode, Execute, Memory access, and Register write
 - Incorporates single cycle DSP function Multiply-Accumulate (MAC)
 - Memory Management Unit (MMU)
 - Built-in Debug Support Unit (DSU)
 - Support of Big/Little Endian modes
- Maximum Operating Frequency: 133MHz
- Power Supply: $V_{DD} = 3.3V$ (I/O), 2.5 (internal)
- Package: 240-pin QFP

Peripheral Features

- SDRAM Controller
 - Supports up to 8 channels of SDRAM, Flash (DIMM), SGRAM, or SMROM memory
 - Supports 16M/64M/128M/256M bit SDRAM with 2/4 bank memory size availability
 - Supports either SDRAM, DIMM Flash, SMROM, SGRAM memory on each channel
 - Support of 16/32-bit wide memory bus sizing
 - Supports Single Data Rate (SDR) SDRAM
 - Supports JEDEC standard 100 or 168-pin memory DIMMs for SDRAM
 - Supports JEDEC standard 100-pin memory DIMM for Flash
- ROM Controller
 - Supports up to 8 independent channels of ROM controller with a single chip select per channel

- Supports various memory sizes of 1M Byte to 1GByte per channel
- Supports independent per channel 16/32-bit static bus sizing and fast page read mode
- Supports ROM, Page Mode ROM, Mask ROM, EPROM, E²PROM, SRAM, and Flash Memory
- Timer/Counter
 - 3-channel 24-bit up-counter
 - Interval and Watchdog timer modes
 - Support up to 3 external timer output pins
 - Support of external input clock
- Interrupt Controller
 - Priority process of 8 internal and up to 6 external interrupt sources
 - Support of Non-Maskable Interrupt (NMI)
- PCI Controller
 - Full compliance with PCI Local Bus Specification Rev. 2.1
 - 32-bit PCI interface at 33MHz
 - 3.3V operation, 5V tolerant buffers
 - Supports both target and initiator mode
 - Supports zero-wait-state read and write burst transfer for target mode
 - FIFO to minimize initial latency requirements to and from memory controller
 - Arbitrator function can be enabled/disabled
 - External interrupt function capability
- Direct Memory Access Controller (DMAC)
 - Independent 4-channel DMA
 - Supports 8/16/32-bit wide I/O devices
 - Supports Internal/External transfer requests
 - Supports both Dual Address and Single Address transfer modes
 - Support of word aligned memory to memory transfers using 4-word/8-word burst read and writes
- Serial I/O Ports
 - Two-channel UART
 - Baud rate generator and modem flow control
- Parallel I/O Ports
 - Supports up to 16 bi-directional I/O pins that can read regardless of direction or mode
 - Support of 16-bit Flag register available as read/write register or Flag register
 - Independent selection of direction of pins and choice of totem-pole or open-drain outputs

TMPR3927F 32-bit MIPS RISC Microprocessor

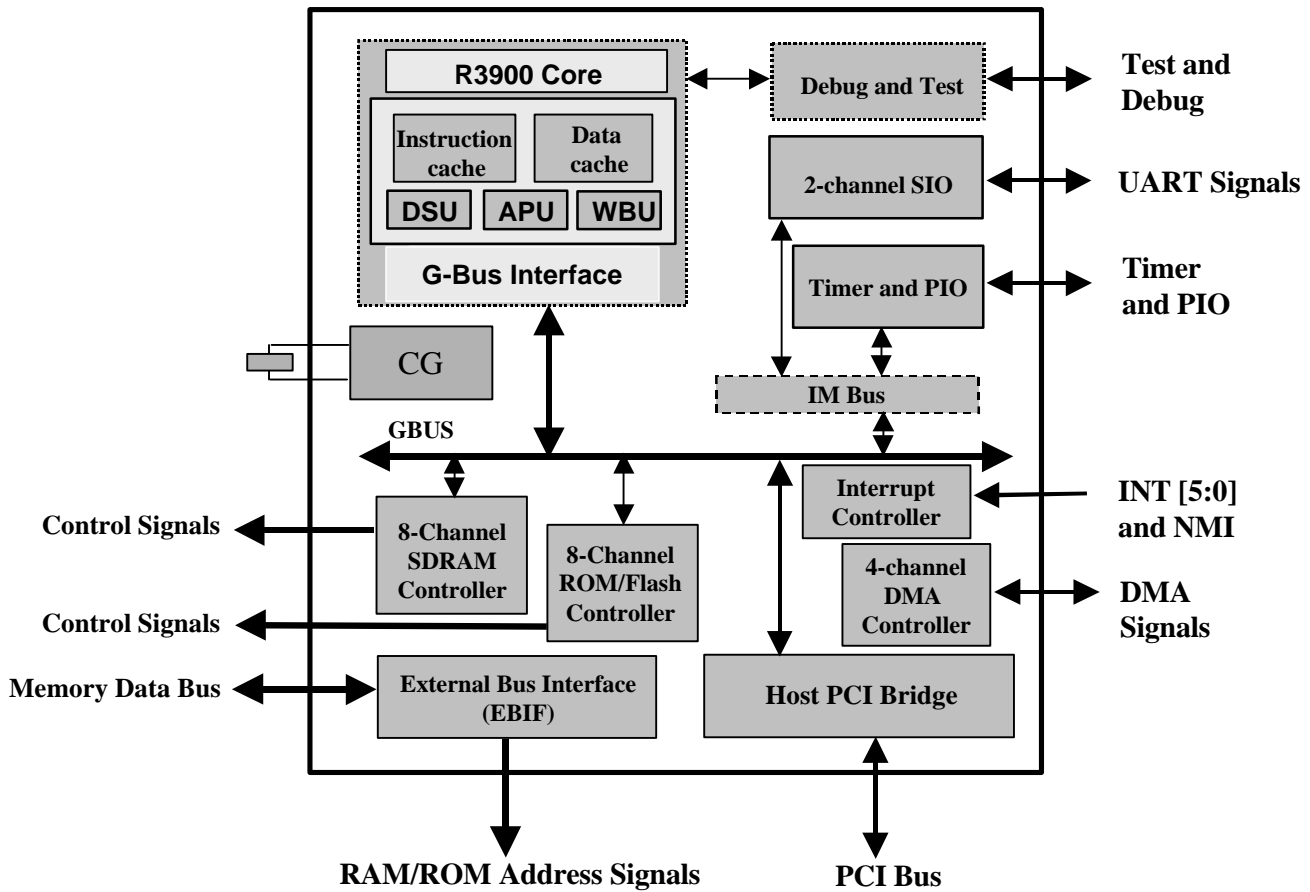


Figure 1. TMPR3927F Block Diagram

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