

[12] Additional Functions

1. Service Pin

The service pin is used during configuration, installation, and maintenance of a LONWORKS node. The pin has both output and input functions. As an output, the service pin is driven active-low to light an external LED. The LED is lit when the node has no valid application code, or when there is an on-chip failure. The LED blinks at a 1/2 Hz rate when the node has not been configured with network address information. A logic-low input at the service pin causes the Neuron Chip to transmit a network management message on the network, containing its own 48-bit Neuron ID. To accomplish both of these functions, the pin is multiplexed between input and output at a 76 Hz rate with a 50% duty cycle (see Figure 1.1). The service pin has an optional on-chip pull-up to bring the input to an inactive-high state for use when the LED and pull-up resistor are not connected.

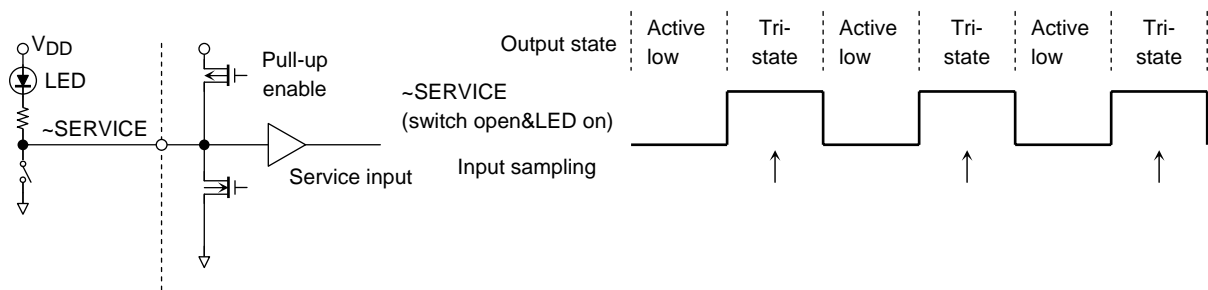


Figure 1.1 Service Pin Circuit

2. Sleep/Wake-Up Circuitry

The Neuron Chip may be put into a low-power sleep mode under software control. In this mode, the oscillator, system clock, communications port, and all timer/counters are turned off, but all state information (including the contents of on-chip RAM) is retained. Normal operation resumes when an input transition occurs on any one of the following pins:

Service pin (not maskable)

I/O pins (maskable):

Any one from IO4 through IO7, selected by the timer/counter multiplexer

Communications port (maskable):

Single-Ended Mode -CP0

Differential Mode -CP0 or CP1

Special-Purpose-mode -CP3

The application software may optionally specify that the programmable pull-ups on the service pin and on I/O pins IO4 to IO7 are to be disabled to further reduce power consumption.

While sleeping, the I/O pins and service pin retain the state they had just before sleep was invoked. For example, if IO [7:0] were outputting a byte of data, that byte remains on these pins for the duration of sleep.

If the communications port is transmitting a packet when the application attempts to put the Neuron Chip to sleep, the Neuron Chip waits until the packet has been sent before going to sleep.

The \sim E pin is held inactive (high) during sleep to disable memory operations during this period. The address bus is driven high (0xFFFF) during sleep to de-select all external devices. The data bus is in the output state (retaining the last value it had just before going to sleep) to keep the data lines from floating and to conserve the need for additional current.

When a wake-up event is detected (a transition on the service pin, selected I/O pin, or communications port wake-up pin), the Neuron Chip allows the oscillator to startup, waits for it to stabilize, performs internal maintenance, and then resumes operation. Typical oscillator start-up times are discussed below (in section 5, *Clocking System*). After the oscillator has started up, the Neuron Chip allows up to 15 transitions on CLK1 for the oscillator to stabilize.

The amount of time required for the Neuron Chip to perform internal maintenance after waking up, before it resumes execution of the application, depends on several application parameters and on whether the Network CPU is servicing application timers during this period. In this respect the most important application parameters are the comm ignore option (see *neuron programmer's guide*), the number of receive transactions (if comm ignore is used), and the number of application timers (if the Network CPU services the application timers during this period).

If the “comm ignore option” is not used, the Neuron Chip typically requires about 2000 CLK1 cycles to perform internal maintenance, and the worst case is about 47,000 CLK1 cycles. The typical case assumes that the Network CPU does not service the application timers during this period. The worst case assumes that the Network CPU must service the maximum number of application timers (15) during this period.

If the “comm ignore option” is used, the Neuron Chip typically requires about 7200 CLK1 cycles for internal maintenance, and the worst case is about 66,000 CLK1 cycles. The typical case assumes that 4 receive transactions are specified, and that the Network CPU does not service the application timers during this period. The worst case assumes that the maximum number of receive transactions (16) are specified, and that the Network CPU must service the maximum number of application timers (15) during this period.

3. Watchdog Timer

The Neuron Chip CPUs are protected against malfunctioning software or memory faults by three watchdog timers (one per CPU). If application or system software fails to reset these timers periodically, the entire Neuron Chip is automatically reset. The watchdog period is approximately * 0.84 seconds at maximum input clock rate (10 MHz) and scales inversely with the input clock rate. When the Neuron Chip is in sleep mode, all the watchdog timers are suspended.

*: When a product supporting an input clock of 20 MHz operates at a 20-MHz clock, the watchdog cycle is about 0.42 second.

4. Reset Circuit

The RESET pin for the Neuron Chip (\sim RESET) is configured for an I/O circuit having open-drain output with an internal pull-up resistor. When the reset pin is held at a voltage of at least 20 ns and less than 0.8 V, the reset operation begins.

The internal RESET circuit for TMPN3150B1AF/3120B1AM/3120E1M, Neuron Chip, TMPN3120FE3M and TMPN3120A20M/A20U/FE5M are shown as Figure 4.1, Figure 4.2 and Figure 4.3.

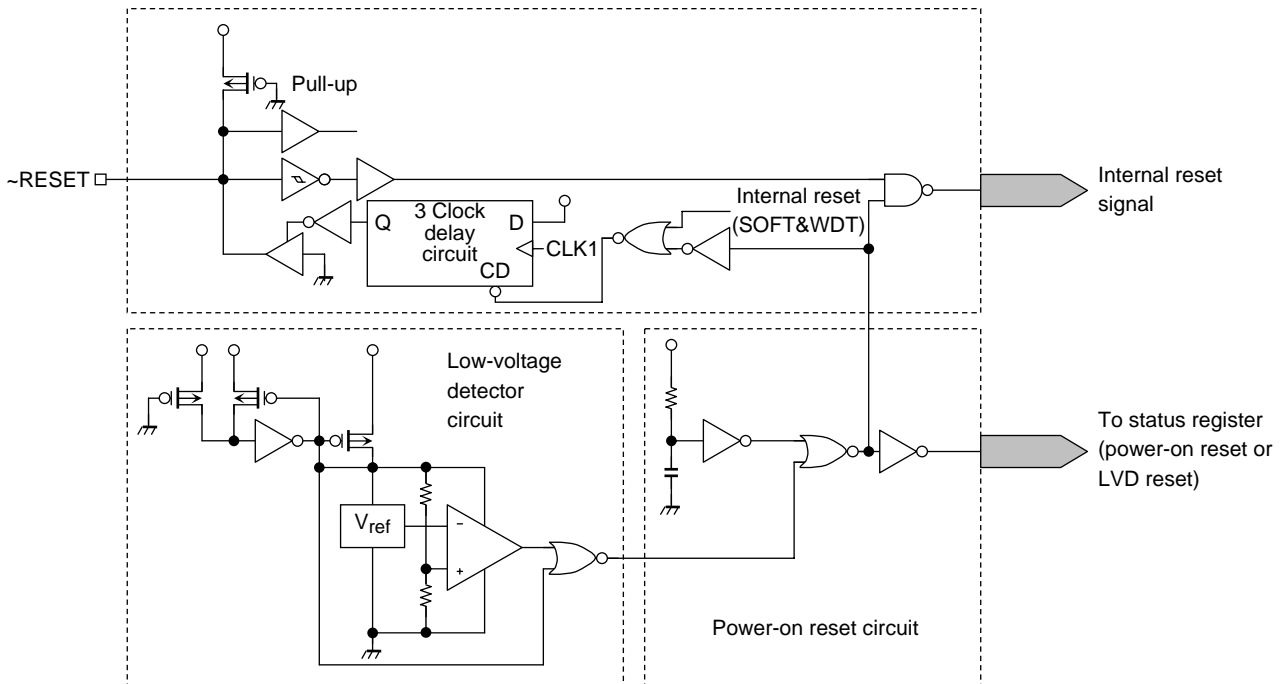


Figure 4.1 Internal RESET Circuits for TMPN3150B1AF/3120B1AM/3120E1M

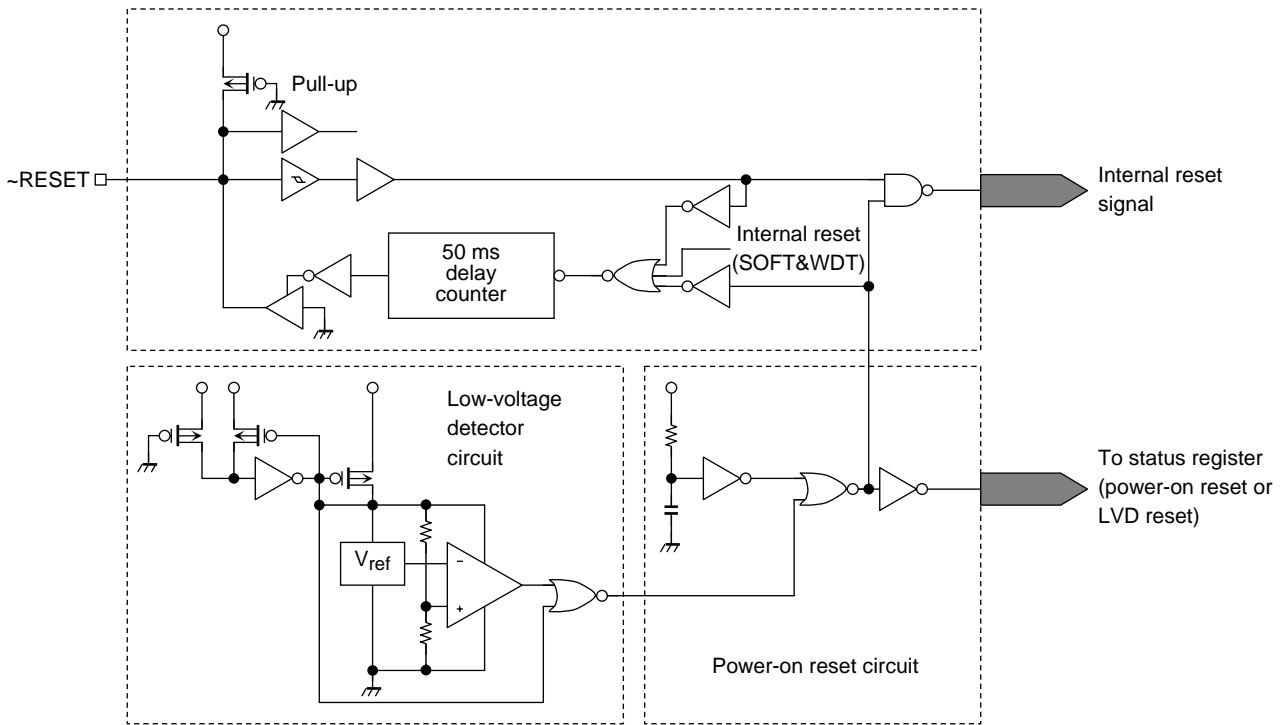


Figure 4.2 Internal RESET Circuits for TMPN3120FE3M

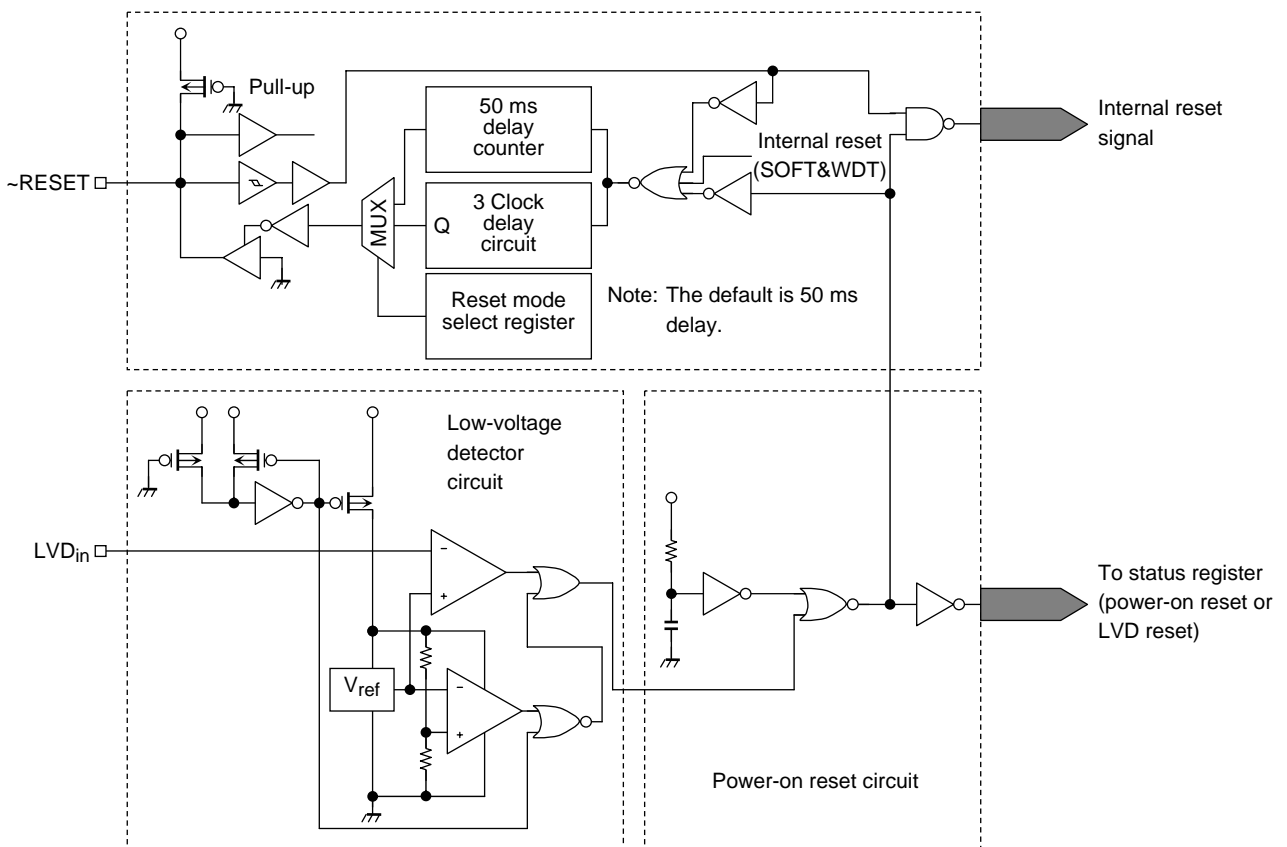


Figure 4.3 Internal RESET Circuits for TMPN3120A20M/A20U and TMPN3120FE5M

The LVD (low voltage detector) circuit is incorporated in the reset circuits shown in Figure 4.1 to Figure 4.3. When the supply voltage (V_{DD}) is less than the threshold value (V_{LVD}), the \sim RESET pin is set low and internal reset signals are generated simultaneously. The LVD reset, the internal software reset the watchdog timer (WDT) reset, and the internal power-on reset signals drive the \sim RESET signals low, and then the \sim RESET pin is held for three clock cycles ($3 \times CLK1$) by the internal three-clock delay circuits or held about 50 ms at least by the 50 ms delay counter. This creates the reset signal hold time for external devices in the case of reset operations for external devices from Neuron Chip \sim RESET signals. When such a reset hold time is insufficient, or in order to protect the reset operation from interference, the \sim RESET pin should be connected to ground through capacitor C_e . Refer to Figure 4.4, where the C_e and the external reset are shown to be connected to the \sim RESET pin. When the Neuron Chip outputs reset signals, the C_e capacitor needs to be discharged, so make sure that it does not exceed 1000 pF.

In the case that Neuron Chip is accidentally reset due to noise, adding external pull-up resistor to \sim Reset might be one of measures to prevent it.

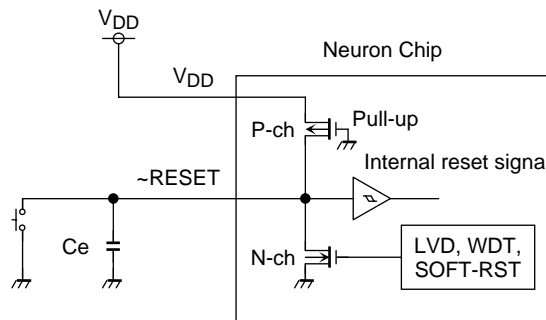


Figure 4.4 Neuron Chip Reset Circuit

The above circuit is sufficient when TMPN3120 $\times\times$, which incorporates an LVD circuit, operates by itself at 10 MHz or less. However, when a product which supports an input clock of 20 MHz operates at 20 MHz, or when as in the case of TMPN3150B1A external memory directly drives operation of the Neuron Chip, an external circuit such as LVD circuit may be required.

When connecting external LVD or LVI (low voltage interrupt), open-drain or open-collector type devices must be directly connected to the \sim RESET pin of the Neuron Chip.

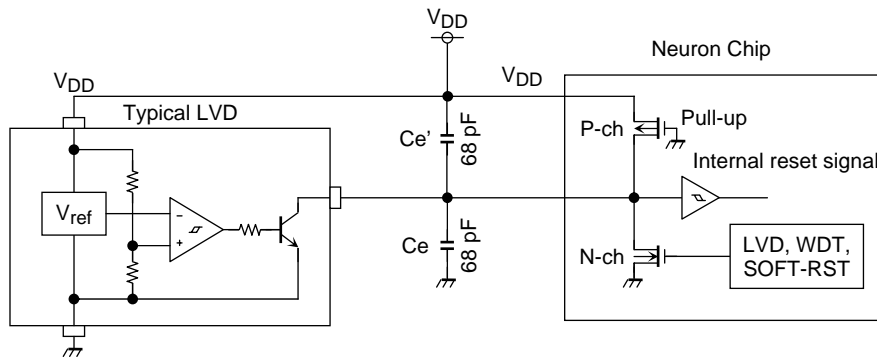


Figure 4.5 External ReACset Circuit with Low-Voltage Detection

Typical low-voltage detector devices include the Mitsumi PST572 series, the Motorola MC34064 and MC34164, and the Dallas Semiconductor DS1233 series. Select any of them after determining the trip point reset voltage, etc.

Conditions for external LDV:

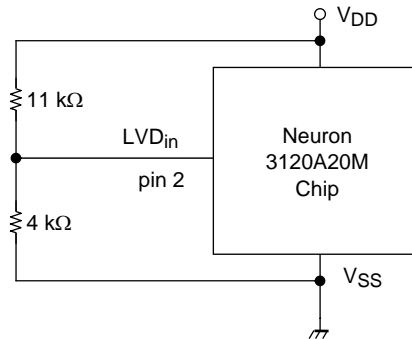
1. Open-drain or open-collector type
2. Minimum operational voltage: $V_{DD} \leq 1.5 \text{ V}$
3. Reset pulse stretching type (when using external EEPROM)

5. Programmable Low Voltage Detection

The existing low voltage detector (LVD) on the Neuron Chip trips whenever the V_{DD} input is less than 4.15 ± 0.35 V. The programmable LVD feature allows the user to select a higher trip voltage if necessary. One of the V_{DD} pins of the 3120 chips is reassigned as the LVD control pin (LVD_{in}). The programmable LVD trips if the LVD_{in} input is below 1.2 ± 0.2 V or V_{DD} is below 4.15 ± 0.35 V. This behavior is backward compatible with earlier Neuron Chips; if the LVD_{in} input is connected to V_{DD} , only the 4.15 V LVD is operational. The LVD_{in} is pin 2 for the SOP-32 package, pin 41 for the QFP-44 package.

Example 1

Increasing Default LVD Trip Point



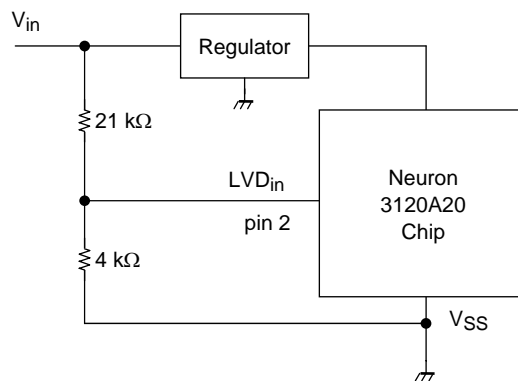
The voltage divider sets the LVD_{in} voltage to $V_{DD} \times 4 / (11 + 4)$

The LVD_{in} trip point is 1.2 ± 0.2 V. This translates to a V_{DD} trip point of 4.5 ± 0.75 V.

Note: TMPN3120A20A20U/M and TMPN3120FE5M only have the programmable low voltage detection.

Example 2

Early Warning Low Voltage Detection



The voltage divider sets the LVD_{in} voltage to $V_{in} \times 4 / (21 + 4)$

The LVD_{in} trip point is 1.2 ± 0.2 V. This translates to a V_{DD} trip point of 7.5 ± 1.25 V.

6. Reset Processes and Timing

Asserting the \sim RESET pin causes the Neuron Chip to perform a fixed set of hardware and firmware initialization tasks. These tasks configure the state of the Neuron Chip pins and memories so that it is ready to begin execution of the application. These tasks and their effects on the Neuron Chip pins are shown in Figure 4.5 The tasks are:

- Oscillator Start-up
- Oscillator Stabilization
- Stack Initialization and Built-in Self-Test
- Service Pin Initialization
- State Initialization
- Off-Chip RAM Initialization
- Random Number Seed Calculation
- System RAM Setup
- Communications Port Initialization
- Checksum Initialization
- One Second Timer Initialization
- Scheduler Initialization

During oscillator start-up, the Neuron Chip allows the oscillator enough time to create a signal swing of greater than approximately 1.7 volts. This duration depends on the type of oscillator used and its frequency (see section 6). This period begins as soon as power is applied to the oscillator, and is independent of the \sim RESET pin. The oscillator start-up period may end before or after \sim RESET is released, depending on the duration of reset and on the time required by the oscillator to start up.

Oscillator stabilization begins when both the \sim RESET pin has released, and the oscillator has started up. The Neuron Chip waits for up to 15 transitions on CLK1 to allow the oscillator's frequency to stabilize. From the time \sim RESET is asserted until the end of the oscillator stabilization period, the I/O pins, communications port pins, and \sim SERVICE pin are in a high-impedance state. The \sim E signal goes inactive (high) immediately after \sim RESET goes low, and the address bus becomes high (0xFFFF) to de-select external devices. **Note that pulling the \sim RESET pin low externally while \sim E is low could result in the \sim E signal going high prematurely. For external devices that depend on a full low duration of the \sim E signal, the external reset signal should be synchronized with the rising edge of \sim E.**

The Stack Initialization and Built-in Self-Test Task tests the on-chip RAM, the timer/counter logic, and the counter logic. If the RAM fails its self-test, the node goes offline, the Service LED comes on solid, and an error is logged in the node status structure (see the query status command description in section B.12). To pass the test, all three CPUs as well as the ROM must be functioning. A flag is set to indicate whether the Neuron Chip passed or failed the Built-in Self-Test. The RAM is cleared to all 0's by the end of this step. At the beginning of this task, the pull-ups on IO [7:4] are enabled so that a weak high state can be observed on these pins. The \sim SERVICE pin oscillates between a solid low a weak high. The memory interface signals reflect execution of these tasks.

The Service Pin Initialization Task simply turns off the \sim SERVICE pin and disables IO [7:4] pull-ups.

The State Initialization Task determines if a Neuron Chip boot is required, and if so, performs it. The Neuron Chip decides to perform a boot if the boot ID is blank, if the boot ID does not match the boot ID in ROM (for the TMPN3150 chip only), or if the reboot word in ROM (defined by the LonBuilder export process) specifies such action. Refer to the *LonBuilder User's Guide* for more information on the reboot word.

When data at the specific address in EEPROM are 0X00 or 0XFF, the Neuron Chip decides that the data are blank. The byte is at offset 0X09 in the configuration structure (appendix A.6).

The boot ID consists of two bytes starting at 0xF1FE which are set to the boot ID in ROM during the boot process. The user can force a boot process to begin by clearing these two bytes and then resetting the Neuron Chip.

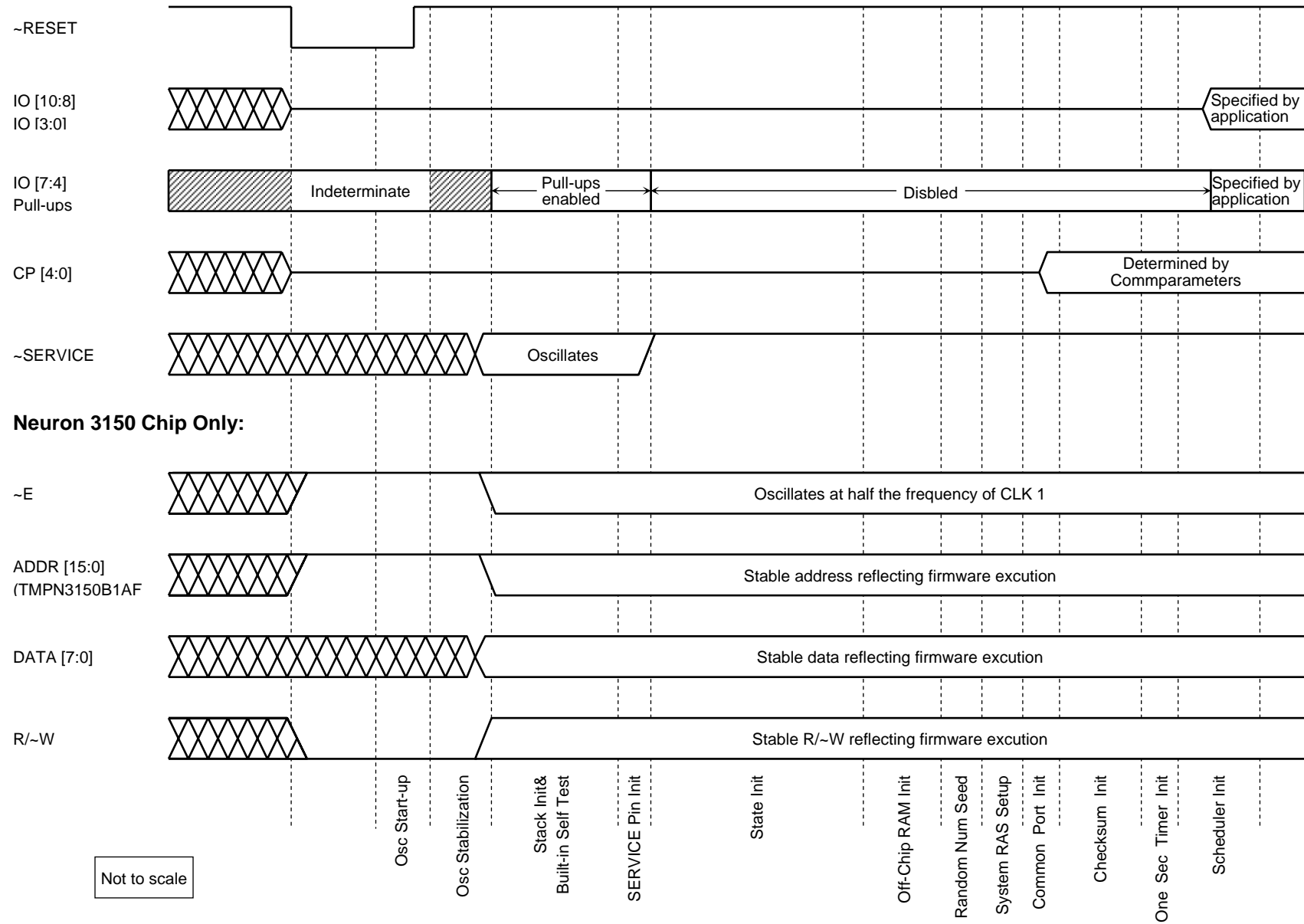


Figure 6.1 Reset Timing

The boot process varies according to the particular model of Neuron Chip being used. For the TMPN3120×× Chips, it simply copies the default communication parameters and mode table from ROM into EEPROM. For the TMPN3150 Chip, it copies a variable amount of data from ROM to EEPROM. The amount of data varies as a function of the target state of the node. If the node is to come up applicationless, the boot process is the same as that for the TMPN3120 Chip. To come up in either the configured or unconfigured state, the boot process must also copy the configuration and code areas of on-chip EEPROM which can vary from 64 to 504 bytes.

The Off-Chip RAM Initialization Task checks the memory map to determine if any off-chip RAM is present, and then either tests and clears all of the off-chip RAM or, optionally, only clears the application RAM area. This choice is controlled by the application program via a Neuron C pragma statement. This task applies only to the TMPN3150 Chip.

The Random Number Seed Calculation Task creates a seed for the random number generator.

The System RAM Setup Task sets up internal system pointers as well as the linked lists of system buffers.

The Communications port Initialization Task initializes the communications port according to the application-specified communications port parameters, and the MAC Processor begins handling packets. For Special-Purpose mode, the configuration registers are initialized.

The Checksum Initialization Task generates or checks the checksums of the non-volatile writeable memories. If the boot process was executed for the configured or unconfigured states, in the State Initialization Task, then new checksums are generated; otherwise, they are only checked. This process includes on-chip EEPROM, off-chip EEPROM, and off-chip non-volatile RAM. ROM is not checksummed. There are two checksums, one for the configuration image, and one for the application image.

Note that the application image checksum includes the configuration image; that is, the configuration image is checksummed twice. In each case, the checksum is a negated two's complement sum of the values in the image. See Appendix A for more details on the configuration and application images.

The One-Second Timer Initialization Task initializes the one second timer. At this point, the Network Processor is available to accept incoming packets.

The Scheduler Initialization Task allows the Application Processor to perform application-related initialization procedures as follows:

State Wait-wait for the node to leave the applicationless state.

Pointer Initialization-perform a global pointer initialization.

Initialization Step-execute an initialization task which is created by the compiler/linker, to initialize static variables and the timer/counters.

I/O Pin Initialization Step-initialize I/O pins based on an application definition. Prior to this point, I/O pins are tri-stated.

State Wait II-wait for the node to leave the unconfigured or hard-offline state. If waiting was required, a flag is set to indicate that the node should come up offline.

Parallel I/O Synchronization-nodes using parallel I/O attempt to execute the master/slave synchronization protocol.

Reset Task-execute the application reset task.

If the offline flag was set, go offline and execute the offline task. If the Built-in Self-Test flag indicated a failure, then the Service Pin is turned on and the offline task is executed. Otherwise the scheduler starts its normal task scheduling loop.

The amount of time required to perform these steps depends on many factors, including: Neuron Chip model; input clock rate; whether or not the node performs a boot process; whether the node is applicationless, configured, or unconfigured; amount of off-chip RAM; whether the off-chip RAM is tested, or simply cleared; the number of buffers allocated; and application initialization. Tables 6.1 and 6.2 summarize the number of input clock cycles (CLK1) required for each of these steps, for the TMPN3120B1AM Chip and the TMPN3150 Chip. The times are approximate and are given as functions of the most significant application variables.

Table 6.1 Time Required for the TMPN3120B1M/E1M/A20M/A20U Chip to Perform Reset Sequence

Step	Approximate Number of CLK1 Cycles	Notes
Oscillator Start-up	See Section 5, Clocking System	
Oscillator Stabilization	15	
Stack Initialization and Built-in Self-Test	200,000	
Service Pin Initialization	1000	
State initialization	250 (for no boot) 2,275,000 (for boot)	
Off-Chip RAM Initialization	0	
Random Number Seed Calculation	0	1
System RAM Setup	21,000 + 600*B	2
Communications Port Initialization	0	1
Checksum Initialization	3400 + 175*M	3
One-Second Timer Initialization	6100	
Scheduler Initialization	≥ 7400	4

Note1: These tasks run in parallel with other tasks

Note2: B is the number of buffers allocated

Note3: M is the number of bytes to be checksummed

Note4: Assumes a trivial initialization task, no reset task, and the configured state

For example, the timing of each of these steps is shown below for a TMPN3120B1M/E1M/A20M/A20U Chip application with the following parameters: 10 MHz input clock, crystal oscillator, no boot required, minimum number of buffers, and checksum performed on 500 bytes of EEPROM.

Oscillator Start-up	1.6 ms	(from Table 7.3)
Oscillator Stabilization	0.002 ms	
Stack Initialization and Built-in Self-Test	20 ms	
Service Pin Initialization	0.1 ms	
State Initialization	0.025 ms	
Off-Chip RAM Initialization	0	
Random Number Seed Calculation	0	
System RAM Setup	2.7 ms	
Communications Port Initialization	0	
Checksum Initialization	10.8 ms	
One Second Timer Initialization	0.61 ms	
Scheduler Initialization	<u>0.74 ms</u>	
* Total	36.6 ms	

*: The total is added approximately 10 ms for TMPN3120E1M and TMPN3120A20M/U, added approximately 45 ms for TMPN3120FE3M and added approximately 100 ms for TMPN3120FE5M.

Table 6.2 Time Required for the TMPN3150 Chip to Perform Reset Sequence

Step	Number of CLK1 Cycles	Notes
Oscillator Start-up	See Section 5, Clocking System	
Oscillator Stabilization	15	
Stack Initialization and Built-in Self-Test	425,000	
Service Pin Initialization	1,000	
State Initialization	1,300 (for no boot)	
	325,000 + 25 ms*E (for boot)	1
Off-Chip RAM Initialization	24,000 + 214*R (for test and clear)	2
	24,000 + 152*Ra (for clear only)	3
Random Number Seed Calculation	max 50,000	
System RAM Setup	27,000 + 1500*B	4
Communications Port Initialization	0	5
Checksum Initialization	36,000 + 175*M (for no boot)	6
	82,000 + 100 ms + 175*M (for boot)	6, 7
One-Second Timer Initialization	6,100	
Scheduler Initialization	≥ 7,400	8

Note1: E is the number of non-zero bytes being written (ranges from 10 to 504)

Note2: R is the number of off-chip RAM bytes

Note3: Ra is the number of non-system off-chip RAM bytes

Note4: B is the number of buffers allocated

Note5: These tasks run in parallel with other tasks

Note6: M is the number of bytes to be checksummed

Note7: Only if booting to the configured or unconfigured state; if booting to the applicationless state, use the “no boot” equation

Note8: Assumes a trivial initialization task, no reset task, and the configured state

For example, the timing of each of these steps is shown for a TMPN3150 Chip application with the following parameter: 10 MHz input clock, crystal oscillator, no boot required, 16 Kbytes external RAM, test and clear external RAM, minimum number of buffers, and checksum performed on 500 bytes of EEPROM.

Oscillator Start-up	1.6 ms	(from Table 7.3)
Oscillator Stabilization	0.002 ms	
Stack Initialization and Built-in Self-Test	42.5 ms	
Service Pin Initialization	0.1 ms	
State Initialization	0.13 ms	
Off-Chip RAM Initialization	353 ms	
Random Number Seed Calculation	5 ms	
System RAM Setup	4.2 ms	
Communications Port Initialization	0	
Checksum Initialization	12.5 ms	
One Second Timer Initialization	0.61 ms	
Scheduler Initialization	<u>0.74 ms</u>	
Total	420 ms	

7. Clocking System

The Neuron Chip includes an oscillator that may be used to generate an input clock signal, using an external crystal or ceramic resonator circuit. The transconductance of this oscillator is 2.1 milli-Siemens at minimum. The Neuron Chip may operate over a range of input clock rates from 10 MHz *(20 MHz) down to 625 kHz for low-power applications. The valid input clock frequencies are *20 MHz, 10 MHz, 5 MHz, 2.5 MHz, 1.25 MHz, and 625 kHz. Alternatively, an externally-generated clock signal may drive the CMOS input pin CLK1 of the Neuron Chip, in which case CLK2 should be left unconnected. In this case, set the rise (t_{cr}) and fall (t_{cf}) of the input clock waveform below 20 ns, respectively (refer to Figure 7.2). As for ordinary CMOS inputs, make sure there is no interference when the input waveform rises and falls. Also, limit the waveform duty ratio to within 40 to 60 %. The accuracy of the input clock frequency must remain within bounds of $\pm 1.5\%$ or better (even with temperature and voltage variations) to ensure that nodes correctly communicate on the network.

Check the transceiver manual because some transceivers require higher precision or cannot use a ceramic resonator.

The Neuron Chip divides the input clock by a factor of two, provide a symmetrical on-chip system clock. The system clock is further divided by powers of two to provide clocks for the applications I/O section, the network communications port, and the CPU watchdog timers.

*: Only a product supporting an input clock of 20 MHz

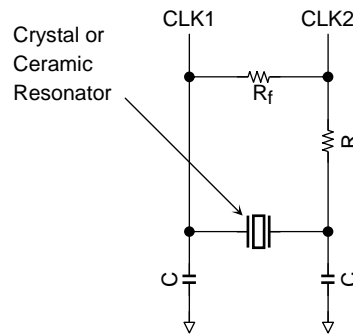


Figure 7.1 Neuron Chip Clock Generator Circuit

Note: The crystal or ceramic resonator needs to be installed as close to the Neuron Chip pin as possible in order to prevent interference from noise or other signals.

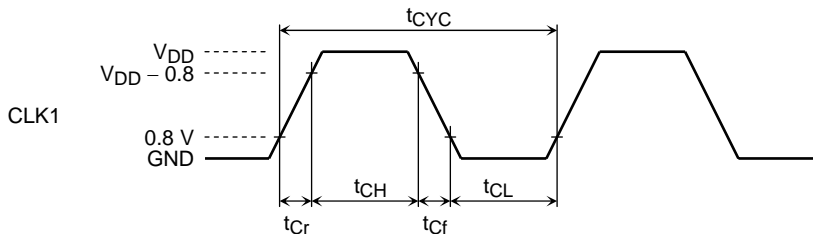


Figure 7.2 Waveform of External Clock Input to NEURON CHIP

Table 7.1 Clock Generator Component Values (see following notes)

Input Clock Frequency	Crystal		Ceramic Resonator	
	R	C	R	C
20.0 MHz (*1)	120 Ω	15 pF	120 Ω	7 pF
10.0 MHz	270 Ω	30 pF	270 Ω	30 pF
5.0 MHz	470 Ω	30 pF	270 Ω	30 pF
2.5 MHz	1.0 kΩ	36 pF	1.0 kΩ	36 pF
1.25 MHz	1.2 kΩ	47 pF	1.2 kΩ	47 pF
0.625 MHz	2.7 kΩ	47 pF	1.2 kΩ	100 pF

*1: These values apply only to products for which a 20-MHz input clock is available. Rf is not connected (provisional value).

Note1: The capacitor values include stray capacitances. Crystal or ceramic resonator manufacturers may recommend other values.

Note2: Rf = 100 kΩ. Rf is required with ceramic resonator configurations. With crystal configurations Rf is not required but may be used.

Note3: Crystal or ceramic resonator frequency = Input clock frequency.

Note4: Crystal may be parallel or series resonant. NPO-type ceramic capacitors are recommended. Resistor and capacitor tolerance is ±5%. Table 6.2 lists a source for the ceramic resonators as an aid in the selection of components.

Table 7.2 Available Ceramic Resonators

Supplier	Murata Electronics North America, INC 2200 Lake Park Drive, Smyrna, GA 30080-7604, USA Phone: 1-770-436-1300 Fax: 1-770-436-3030
20.0 MHz	CSTCE20M0V53-R0
10.0 MHz	CSTCE10M0G55-R0
5.0 MHz	CSTCR5M00G55-R0
2.5 MHz	CSTCC2M50G56-R0
1.25 MHz	CSB 1250J(*2)
0.625 MHz	CSB 625P

Typical start-up times for this clock circuit with the Neuron Chip are shown in Table 7.1. Actual start-up times vary depending on the crystal of the ceramic resonator used.

*2: Exclude TMPN3120A20M/U, TMPN3120FE3M/U and TMPN3120FE5M.

Table 7.3 Typical Start-Up Times

Input Clock Frequency	Crystal	Ceramic Resonator
20.0 MHz (*3)	0.5 ms	8 μs
10.0 MHz	0.5 ms	8 μs
5.0 MHz	1.0 ms	15 μs
2.5 MHz	2.0 ms	30 μs
1.25 MHz	3.0 ms	60 μs
0.625 MHz	10.0 ms	380 μs

*3: These values apply only to products for which a 20-MHz input clock is available.

