

Product Brief

Highlights

- Highly integrated system-on-chip (SoC) for digital TVs that incorporates a high-performance 64-bit RISC processor and two highly optimized DSP processors
- Specifically designed for North American TV standards (ATSC & digital cable)
- Integrated VSB/QAM demodulator for ATSC TV
- Complete reference system with software and middleware support for quick product deployment
- Software and middleware based on Linux® OS
- Common API support for middleware and application development
- Decode single-standard definition stream or single high-definition stream
- Decode one audio stream
- Two 480i or one 720p/1080i analog video outputs and one SD/HD digital video output
- Unified memory architecture for optimum system cost
- Built-in MPEG-2 decoder, high-performance scalar and graphics controller for high-quality video output
- Low-power SoC with power-down modes
- Package: 292-pin PBGA and 256-pin LQFP

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TC90407XBG/FG Single-chip Solutions for Digital TV

Description

The TC90407XBG/FG is the second-generation product from Toshiba targeted for mid- to low-end digital TV applications. Compared to previous designs, it integrates more functional blocks on chip reducing system cost and supports new algorithms for improved picture quality. The device incorporates VSB/QAM logic on chip for ATSC and Cable streams demodulation.

The TC90407XBG/FG is capable of decoding single SD or HD stream and display content in standard-definition resolution (720 x 480 pixels) or half high-definition resolution (960 x 1080 pixels). With two analog and one 8/16-bit digital outputs, the TC90407XBG is a very cost-effective solution for CRT TV, LCD TV or digital-to-analog converter set-top box applications.

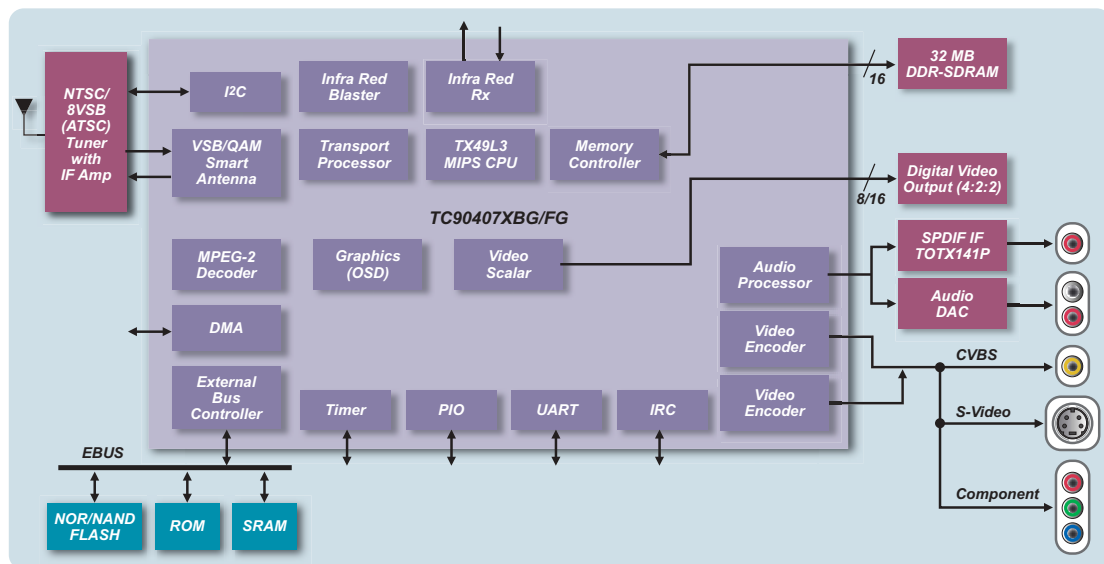
The TC90407XBG/FG devices use multiple DSP engines to perform compute-intensive, multimedia operations to offload the main CPU for efficient system management of

demanding digital TV applications. The TC90407XBG architecture also supports a unified 16-bit DDR memory system, as well as a NAND and a NOR flash memory controller to reduce overall system cost.

Features

- 162 MHz TX49/L3 64-bit MIPS RISC core
 - 8 KB each I & D cache
 - Unified memory system
 - DDR SDRAM controller (16-bit, 162 MHz)
 - NAND & NOR Flash support
- Transport Stream Processor
 - Fully compliant to ATSC and cable transport streams
- Video Decoder (SD decoding)
 - MPEG-2 decoding (MP@ML and MP@SL) and MPEG-1 decoding
 - Single-MPEG-2 decoding
- Video Decoder (HD decoding)
 - MPEG-2 decoding for MP@HL for ATSC
 - Display in HD resolution up to 960 x 1080
 - 720p or 1080i compliant
 - HD-to-SD down-conversion
- Display in SD resolution

TC90407XBG/FG Block Diagram



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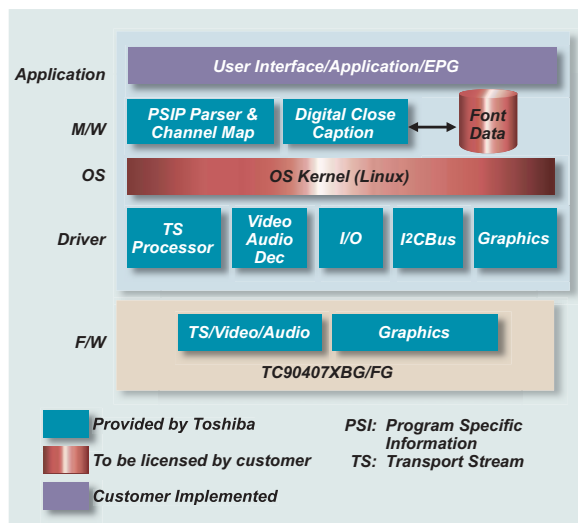
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- Audio Processor
 - MPEG- Audio, Dolby AC-3 decoding
 - I²S and S/P-DIF Transmitter (IEC-60958/61937)
- Graphics Engine
 - Two planes (YUV/Graphics)
 - Alpha blending and video scaling
 - Progressive scan (I/P conversion by line-interpolation)
- Video Output
 - Dual NTSC Video Encoder
 - 4 DACs (supports two 480i analog outputs for SD and one 720p/1080i output for HD)
 - 4:2:2 YUV Digital-Output (ITU R656/R601)
 - VBI re-insertion (closed-caption and CGMS-A)
 - Interlaced or progressive output
- Interfaces and Peripherals
 - 8/16-bit local bus for NAND/NOR flash and other I/O devices (40.5 MHz),
- DMA controller (2 ch), SIO (2 ch), PIO (10), timer/counter (three 24-bit), I²C (2 ch), IR-decoding and IR-blaster
- Power-down and Standby Operations
- Package
 - TC90407XBG – 292-pin PBGA package
 - TC90407FG – 256-pin LQFP package in Q1'07

TC90407XBG Development Tools

- Reference Board: DLVM-GC and DLVM-GL reference modules
- Operating System: Monta Vista Software, Inc.: Monta Vista Linux
- Development Tools: Compilers, debugger and assemblers
- Software Support: Firmware, Device Drivers, ATSC middleware

TC90407XBG/FG Software Structure Diagram



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